

SIMATIC DP, ELECTRONIC MODULE 2 AO HIGH FEATURE U
FOR ET 200S, 15 MM WIDE, +/-10V; 15 BIT + SIGN, 1 .. 5V; 15 BIT,
OPERATIONAL LIMITS +/-0.07% WITH LED SF (GROUP FAULT)

Supply voltage

Load voltage L+

- | | |
|-------------------------------|-------------------------|
| • Rated value (DC) | 24 V; From power module |
| • Reverse polarity protection | Yes |

Input current

- | | |
|---|--------|
| from load voltage L+ (without load), max. | 130 mA |
| from backplane bus 3.3 V DC, max. | 10 mA |

Power loss

- | | |
|------------------|-----|
| Power loss, max. | 2 W |
|------------------|-----|

Address area

Address space per module

- | | |
|----------------------------------|--------|
| • Address space per module, max. | 4 byte |
|----------------------------------|--------|

Analog outputs

- | | |
|---|--------|
| Number of analog outputs | 2 |
| Voltage output, short-circuit protection | Yes |
| Voltage output, short-circuit current, max. | 25 mA |
| Cycle time (all channels) max. | 2.5 ms |

Output ranges, voltage

- | | |
|------------------|-----|
| • 1 V to 5 V | Yes |
| • -10 V to +10 V | Yes |

Connection of actuators

- | | |
|---|---|
| • for voltage output two-wire connection | Yes; Without compensation of the line resistances |
| • for voltage output four-wire connection | Yes |

Load impedance (in rated range of output)

- | | |
|---|--------------|
| • with voltage outputs, min. | 1 k Ω |
| • with voltage outputs, capacitive load, max. | 1 μ F |

Destruction limits against externally applied voltages and currents

- | | |
|--|--|
| • Voltages at the outputs towards MANA | 15 V; max. 15 V continuous; 75 V for max. 1 s (mark to space ratio 1:20) |
| • Current, max. | 50 mA; DC |

Cable length

- | | |
|------------------|-------|
| • shielded, max. | 200 m |
|------------------|-------|

Analog value generation for the outputs

Integration and conversion time/resolution per channel	
<ul style="list-style-type: none"> Resolution with overrange (bit including sign), max. 	16 bit; 1 to 5 V: 14 bit, ± 10 V: 16 bit
Settling time	
<ul style="list-style-type: none"> for resistive load 	0.1 ms
<ul style="list-style-type: none"> for capacitive load 	0.5 ms
<ul style="list-style-type: none"> for inductive load 	0.5 ms
Errors/accuracies	
Output ripple (relative to output range, bandwidth 0 to 50 kHz), (+/-)	0.02 %
Linearity error (relative to output range), (+/-)	0.02 %
Temperature error (relative to output range), (+/-)	0.001 %/K
Crosstalk between the outputs, min.	60 dB
Repeat accuracy in steady state at 25 °C (relative to output range), (+/-)	0.01 %
Operational error limit in overall temperature range	
<ul style="list-style-type: none"> Voltage, relative to output range, (+/-) 	0.07 %
Basic error limit (operational limit at 25 °C)	
<ul style="list-style-type: none"> Voltage, relative to output range, (+/-) 	0.03 %
Isochronous mode	
Isochronous operation (application synchronized up to terminal)	Yes
Interrupts/diagnostics/status information	
Substitute values connectable	Yes; Parameterizable; 0 to 65535 (value range must be within rated range)
Diagnostic messages	
<ul style="list-style-type: none"> Diagnostic information readable 	Yes
<ul style="list-style-type: none"> Short-circuit 	Yes
<ul style="list-style-type: none"> Group error 	Yes
Diagnostics indication LED	
<ul style="list-style-type: none"> Group error SF (red) 	Yes
Parameter	
Remark	7 byte
Diagnostics short-circuit	Disable / enable
Output type/range	deactivated / 1 to 5 V / ± 10 V
Group diagnostics	Disable / enable
Response to CPU/master STOP	Output current and de-energized/substitute a value/keep last value
Potential separation	
Potential separation analog outputs	
<ul style="list-style-type: none"> between the channels 	No

- between the channels and backplane bus
- Between the channels and load voltage L+

Yes

Yes

Permissible potential difference

between MANA and M internally (UISO)

75 V DC/60 V AC

Isolation

Isolation tested with

500 V DC

Dimensions

Width

15 mm

Height

81 mm

Depth

52 mm

Weights

Weight, approx.

40 g

last modified:

08/16/2019